SGS-THOMSON MICROELECTRONICS

TDA8140

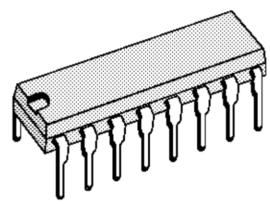
HORIZONTAL DEFLECTION POWER DRIVER

- CONTROLLED DRIVING OF THE POWER TRANSISTOR DURING TURN ON AND OFF PHASE FOR MINIMUM POWER DISSIPATION AND HIGH RELIABILITY
- HIGH SOURCE AND SINK CURRENT CAPABILITY
- DISCHARGE CURRENT DERIVED FROM PEAK CHARGE CURRENT
- CONTROLLED DISCHARGE TIMING
- DISABLE FUNCTION FOR SUPPLY UNDER VOLTAGE AND NONSYNCHRONOUS OPERATION
- PROTECTION FUNCTION WITH HYSTERESIS FOR OVERTEMPERATURE
- OUTPUT DIODE CLAMPING
- LIMITING OF THE COLLECTOR PEAK CURRENT OF THE DEFLECTION POWER TRANSISTOR DURING TURN ON PERIOD
- SPECIAL REMOTE FUNCTION WITH DELAY TIME TO SWITCH THE OUTPUT ON

DESCRIPTION

The TDA 8140 is a monolithic integrated circuit designed to drive the horizontal deflection power transistor.

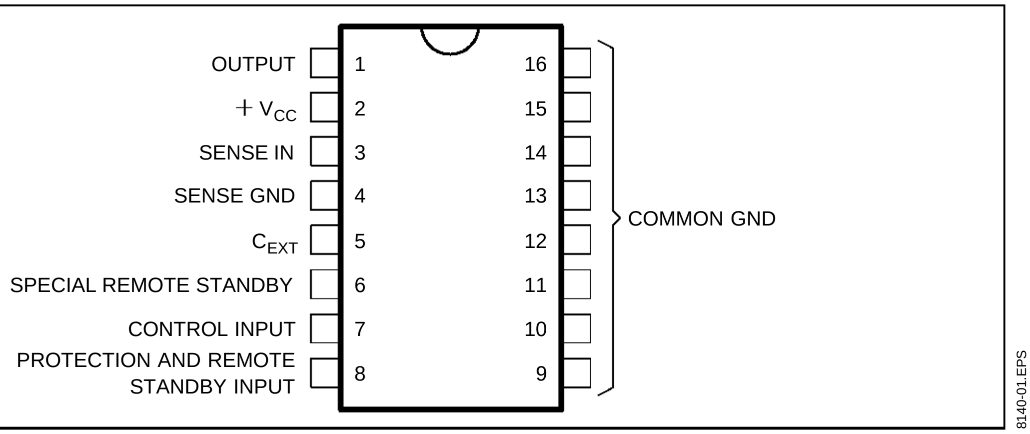
The current source characteristic of this device is adapted to the on-linear current gain behaviour of the power transistor providing a minimum power dissipation. The TDA8140 is internally protected against short circuit and thermal overload.



POWERDIP (8 + 8)
(Plastic Package)

ORDER CODE : TDA8140

PIN CONNECTIONS

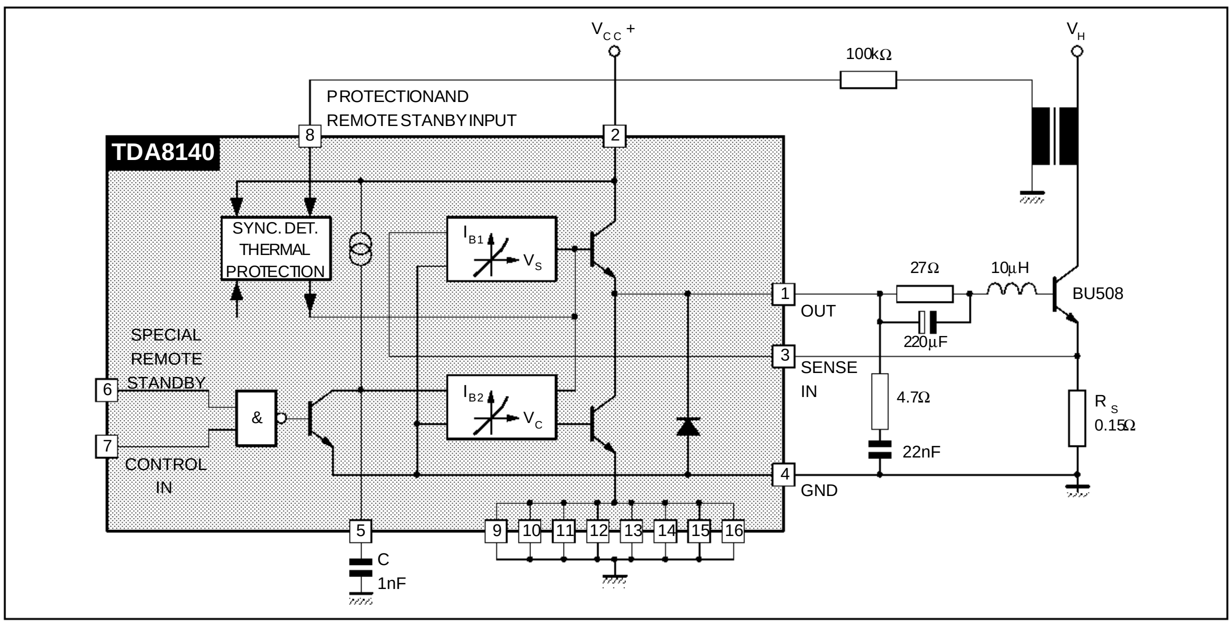


PIN FUNCTION

Pin	Name	Function
1	Output	Device Output
2	V_{CC}	Supply Voltage
3	Sense Input	Input voltage that determines output current.
4	Sense GND	Reference Ground for Input Voltage at Sense Input
5	C_{EXT}	Capacitor between this terminal and Sense Ground determines the current slope dI_o/d_t during off phase.
6	Special Remote/Standby	Low level at this input sets the device after a delay time t_{dr} in the standby mode independent from control input (2nd priority) (in standard applications pin 6 must be left unconnected).
7	Control Input	High level at this input switches the BU508 off, low level switches the BU508 on.
8	Protection and Remote Standby Input	A high level at this input switches the BU508 off independent from all other inputs (1st priority).
9-16	Power Ground	Common Ground

8140-01.TBL

BLOCK DIAGRAM



8140-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	18	V
I_d	Output Current	Internally Limited	
P_{tot}	Power Dissipation	Internally Limited	
T_{stg}, T_j	Storage and Junction Temperature	– 40, + 150	°C
T_{oper}	Operating Temperature	0, + 70	°C

8140-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	15	°C/W

8140-03.TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = 12V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		7		18	V
I_Q	Quiescent Current	All Inputs Open	10	15	25	mA
I_{p0}	Positive Output Current (source)		1.5			A
I_{n0}	Negative Output Current (sink)		2			A
I_{o0}	Positive quiescent output current forcing the output to 6 V and the sense input to ground, output externally forced to 6V	Remote Input 1 Remote Input 0	120 50	150 80	200 100	mA mA
G_{ON}	Transconductance ON Phase (1)	See Figure 1	1.8	2.0	2.2	A/V
G_{OFF}	Transconductance OFF Phase (2)	See Figure 1	1.8	2.0	2.2	A/V
G_{REMOTE}	Transconductance Standby Mode	Remote Input 0	0.675	0.75	0.825	A/V
I_5	Current Source Pin 5	V_6 = 500mV	135	165	200	µA
R_{INS}	Sense Input Resistance	$V_S > 0$ $V_S < 0$	0.7 0.35	1 0.5	1.3 0.7	kΩ kΩ
I_{INS}	Sense Input Bias Current	V_S = 0, Remote Input 1	– 200	– 300	– 400	µA
R_{SYN}	Synchronous Detection Input Resistance	V_{SYN} < 7V V_{SYN} > 7V	30 7	60 10	150 15	kΩ kΩ
V_{THS}	Threshold Voltage of the Synchronous Detection Input		1	1.8	2.8	V
V_{SYN}	Sync Detect Input Voltage				30	V
V_{THA}	Threshold Voltage of Control Input		1.5	2	2.5	V
I_{INA}	Pull up Current of Control Input	$0 < V_{IN} < V_{THA}$ $V_{IN} > V_{THA}$ + 0.5V	– 50 - 1	– 100 0	– 160 + 1	µA µA
V_{THB}	Threshold Voltage Remote Input		1.5	2	2.5	V
I_{INB}	Pull up Current of the Remote Input	$0 < V_{IN} < V_{THB}$ $V_{IN} > V_{THB}$ + 0.5V	– 50 – 1	– 100 0	– 160 + 1	µA µA
t_{dr}	Remote Delay Time (3)		190	250	300	µs
t_{don}	On Delay Time			3	4.5	µs
$V_{CC}–V_{OUT}$	Output Voltage Drop for I_{p0} = 1 A		2	2.8	3	V
$V_{CC\ ON}$	Supply Voltage for Device "ON"	$I_0 \geq 0$	5.8	6.4	7.0	V
$V_{CC\ OFF}$	Supply Voltage for Device "OFF" (output internally switched to ground)		5.6	$V_{CC\ ON}$ – 0.2 V	6.8	V
$V_{S\ limit}$	Sense Limit Voltage (4)		0.8	0.9	1	V

8140-04.TBL

Notes :
1. G_{ON} is measured with V_3 varying from 150mV to 350mV (Pin 5 is grounded)
2. G_{OFF} is measured with V_5 varying from 150mV to 350mV (Pin 3 is grounded)
3. When the remote input goes from HIGH to LOW the BU508 is switched off and it remains in this condition for the time t_{dr}.
4. The sense input voltage V_S is internally limited and results in a limited positive output current I_{p0} = g V_S limit. Note that due to the storage time t_S of the BU508 limiting of V_S leads to a reduced base current of the BU508 and the output current I_0 is going to the positive quiescent current I_{O0}.

TRUTH TABLE

Logic Inputs		Output I_o		Mode
Control Input	Remote/Standby			
0 Floating or 1	Floating or 1 Floating or 1	$I_o > 0$ $I_o < 0$ (5)	BU508 ON BU508 OFF	Normal Function
X	0	$I_o < 0$ (5) $0 < t < t_{dr}$	BU508 OFF	Remote/Standby Function
X	0	$I_o > 0$ $t > td_r$	BU508 ON	

8140-05.TBL

Note : 5. $I_O < 0$ means that the sink current flows into the output to ground.

Figure 1 : $\frac{G_{ON}}{V_{Pin3}}$ and $\frac{|G_{OFF}|}{V_{Pin5}}$

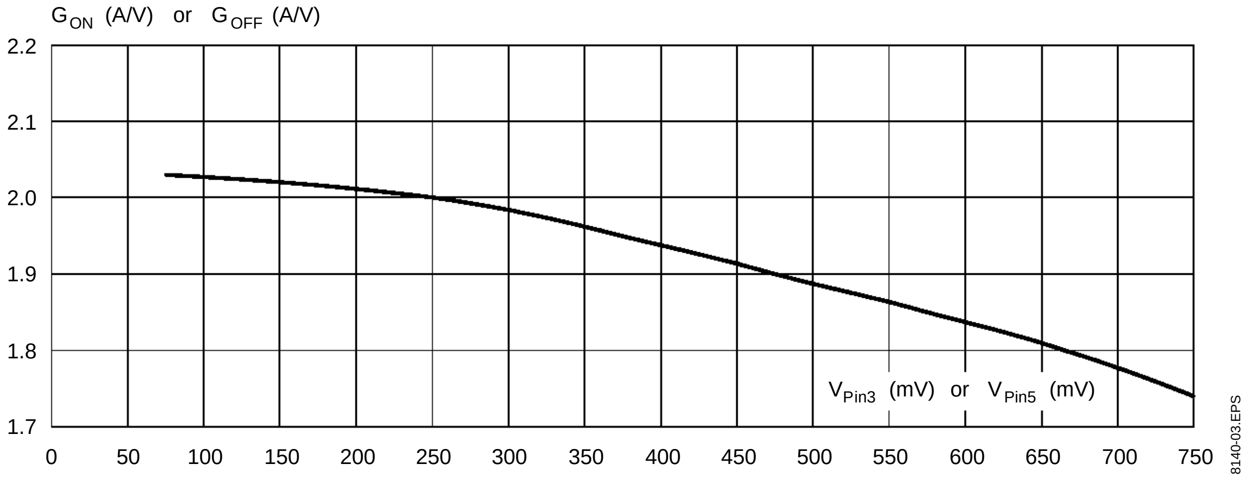


Figure 2 : Large Screen Application

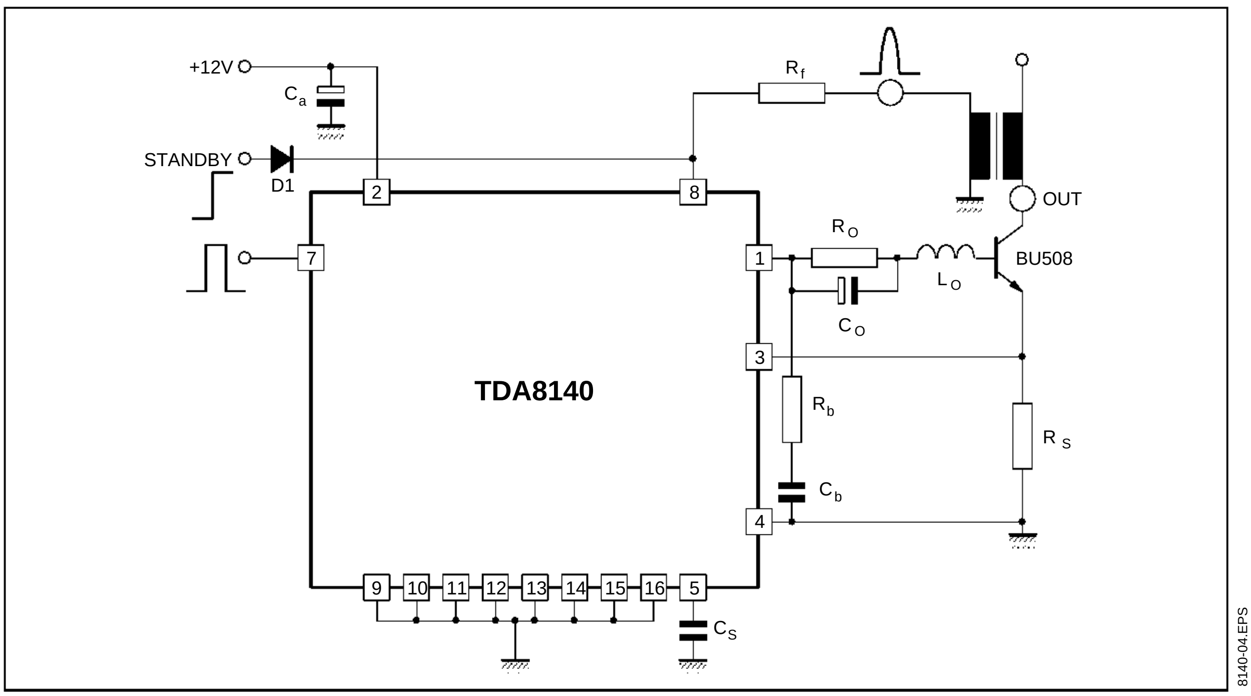
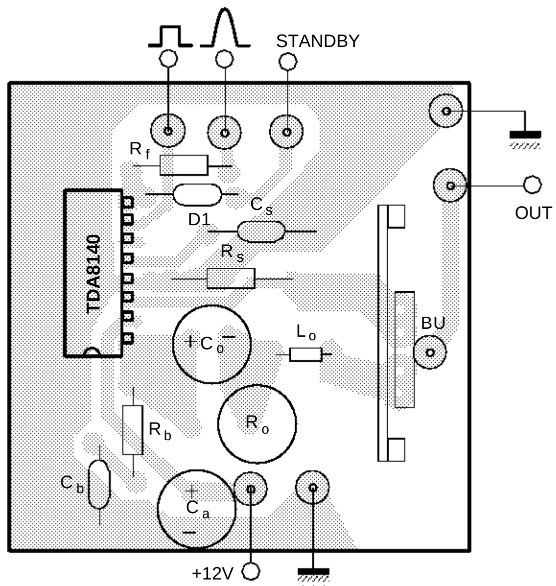


Figure 3 : P.C. Board and Components Layout of the Figure 2 (1 : 1 scale)



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COMPONENTS LIST FOR TYPICAL APPLICATION

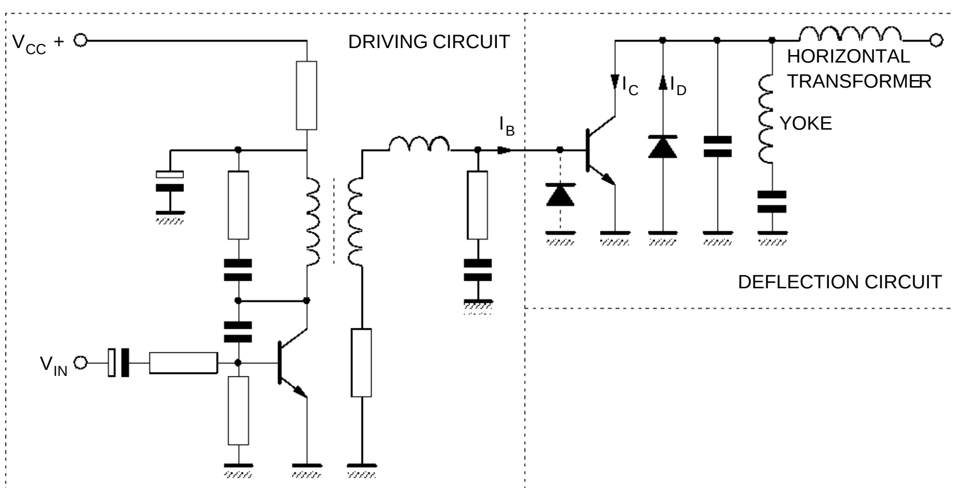
CRT	22"/26" 100°	14"/20" 90°	CRT	22"/26" 100°	14"/20" 90°
C_a	47 µF	47 µF	R_b	4.7 Ω	4.7 Ω
R_o	27 Ω 2W	27 Ω 1 W	C_b	47 nF	47 nF
C_o	220 µF	220 µF	R_s	0.15 Ω	0.1 Ω
L_o	10 µH	10 µH	C_s	1 nF	1 nF

8140-06.TBL

APPLICATION INFORMATION

The conventional deflection system is shown in Figure 4. The driving circuit consists of a bipolar power transistor driven by a transformer and a medium power element plus some passive components.

Figure 4 : Conventional Horizontal Deflection System for TVs



8140-06.EPS

During the active deflection phase the collector current of the power transistor is linearly rising and the driving circuitry must be adapted to the required base current in order to ensure the power transistor saturation.

According to the limited components number the typical approach of the present TVs provides only a rough approximation of this objective ; in Figure 5 we give a comparison between the typical real base current and the ideal base current waveform and the collector waveform.

The marked area represents a useless base current which gives an additional power dissipation on the power transistor.

Furthermore during the turn-ON and turn-OFF transient phase of the chassis the power transistor is extremely stressed when the conventional network cannot guarantee the saturation ; for this reason, generally, the driving circuit must be carefully designed and is different for each deflection system.

The new approach, using the TDA 8140, overcomes these restrictions by means of a feedback principle.

As shown in Figure 5, at each instant of time the ideal base current of the power transistor results from its collector current divided by such current gain which ensure the saturation ; thus the required base current I_b can be easily generated by a feedback transconductance amplifier g_m which senses the deflection current across the resistor R_s at the emitter of the power transistor and delivers :

$$I_b = R_S \cdot g_m \cdot I_e$$

The transconductance must only fulfill the condition :

$$\frac{1}{1+\beta min} \cdot \frac{1}{R_S} < gm < \frac{1}{R_S}$$

Where β_{min} is the minimum current gain of the transistor. This method always ensures the correct base current and acts time independent on principle.

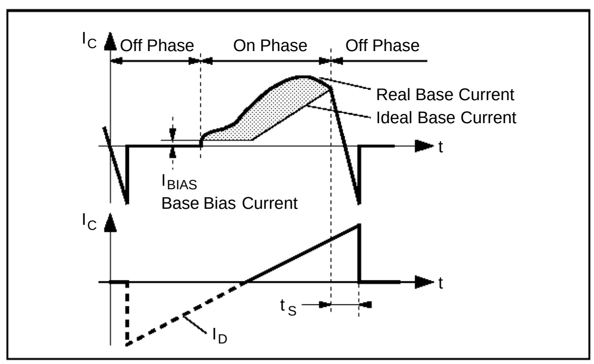
For the turn-OFF, the base of the power transistor must be discharged by a quasi linear time decreasing current as given in Figure 6.

Conventional driver systems inherently result into a stable condition with a constant peak current magnitude.

This is due to the constant base charge in the turn-ON phase independent from the collector current ; hence a high peak current results into a low storage time of the transistor because the excess base charge is a minimum and vice versa. In the active deflection the required function, high peak current-fast switch-OFF and low peak current-slow switch-OFF, is obtained by a controlled base discharge current for the power transistor ; the negative slope of this ramp is proportional to the actual sensed current.

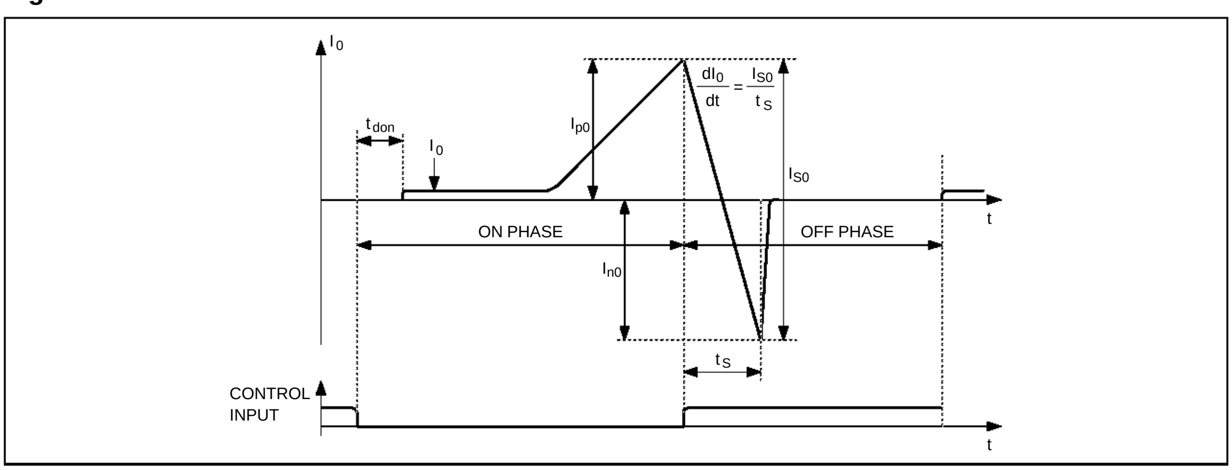
As a result, the active driving system even improves the sharpness of vertical lines on the screen compared with the traditional solution due to the increased stability factor of the loop represented as the variation of the storage time versus the collector peak current.

Figure 5 : Waveforms of Collector and Base Current



8140-07.EPS

Figure 6



8140-08.EPS

CIRCUIT DESCRIPTION

Figure 7 shows the block diagram of the TDA8140, the circuit consists of an input transconductance amplifier composed by Q1, Q2, Q3 and Q4.

The symmetrical output current is fed into the load resistor R1 and R2 ; the two amplifiers V1 and V2 realize a floating voltage to current converter which can drive 1.2A sink current and 2A source current for a wide common output range.

So, the overall transconductance results into :

$$g_m = \frac{R1 + R2}{R3} \cdot \frac{1}{R5}$$

A current source I_1 generates a drop of 70mV across the resistor R4 which provides an output bias current of 140mA; the control input determines the turn ON/OFF function.

In the ON phase, Q5 shorts the external capacitor C_t. Within the input voltage range $0 < V_{in} < 750mV$ the element realizes the transconductance function ; lower voltages are clamped by the D1/Q6 configuration.

For input voltages higher than 750mV, Q7 limits the maximum output current at 1.5A peak.

In the turn-OFF mode, C_t will be charged by the controlled source I_2 which is proportional to the input voltage, by this way, the output current decreases quasi linearly and the system stability is reached.

During the flyback phase, the IC is disabled via the sync. detector input ; this function with the limited sink and source current together with the undervoltage turn-OFF and a chip temperature sensor ensure a complete protection of the IC.

In Figure 8 is shown the application diagram of the TDA 8140, the few external component and the automatic handling possibility ensures a lower application cost versus the conventional approach shown in Figure 4.

In Figure 9 is shown the currents and voltages waveforms of the driver circuit of Figure 8, as to be seen, the driving charge $Ib \cdot t_{on}$ has been reduced at minimum.

Figure 7 : Block Diagram of the Integrated Horizontal Driver

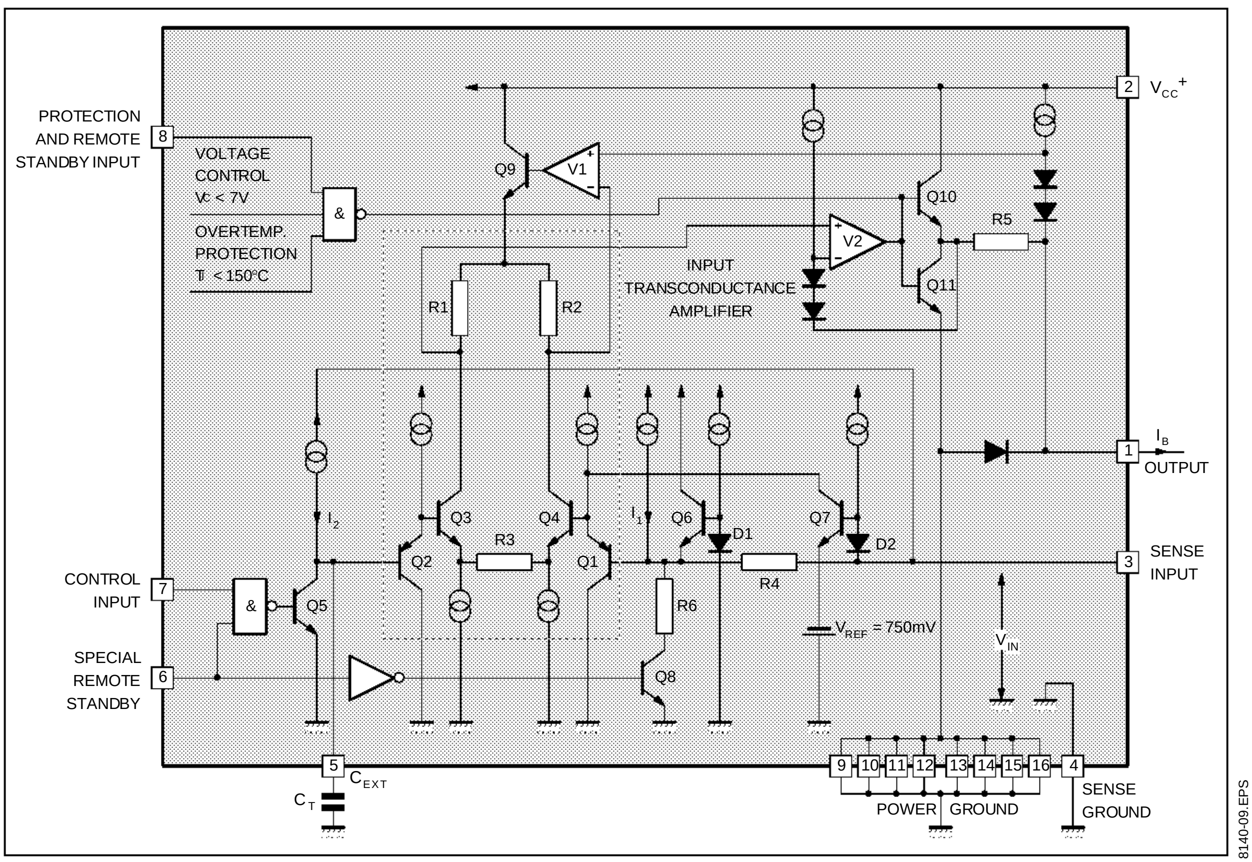


Figure 8 : Integrated Horizontal Driver

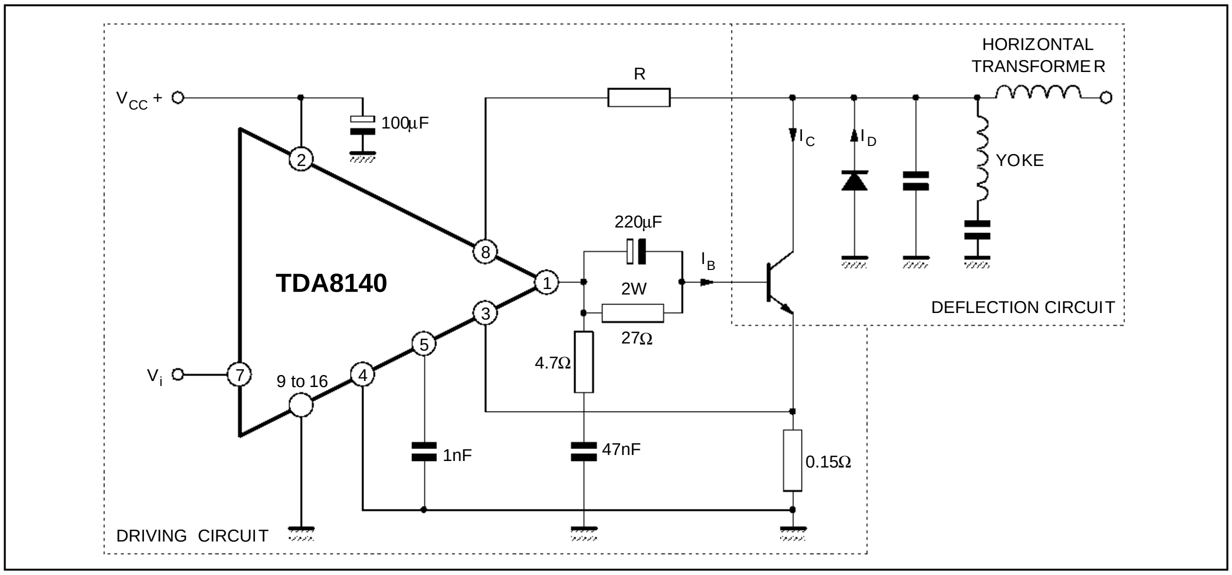
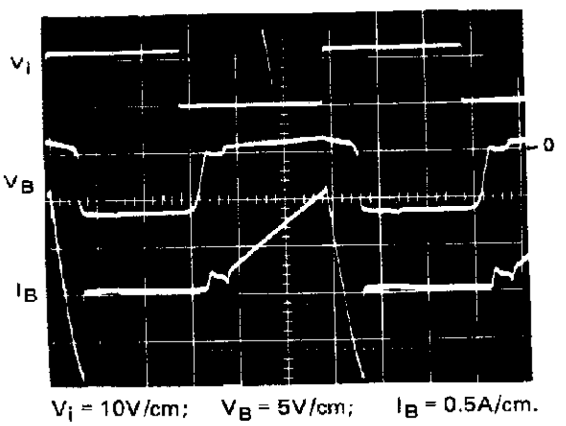
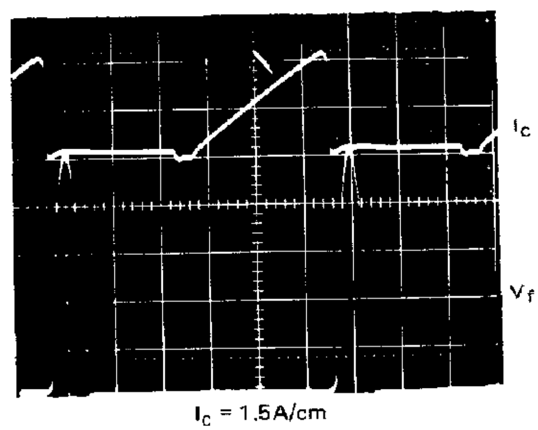


Figure 9 : Signal Diagrams of the Driver Circuits





The power dissipation on this application condition is about 1.3W and Figures 10 and 11 show two ways of heatsinking.
In the first case, a PCB copper area is used as a heatsink L= 65mm while in the second case, the device is soldered to an external heatsink ; in both examples, the thermal resistance junction ambient is 35°C/W.

The presence of thermal shut-down circuit does mean that the heatsink can have a smaller factor of safety compared with that of a conventional circuit.

If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply switches off the device.

Figure 10 : Example of Heatsink using P.C. Board Copper (L = 65mm)

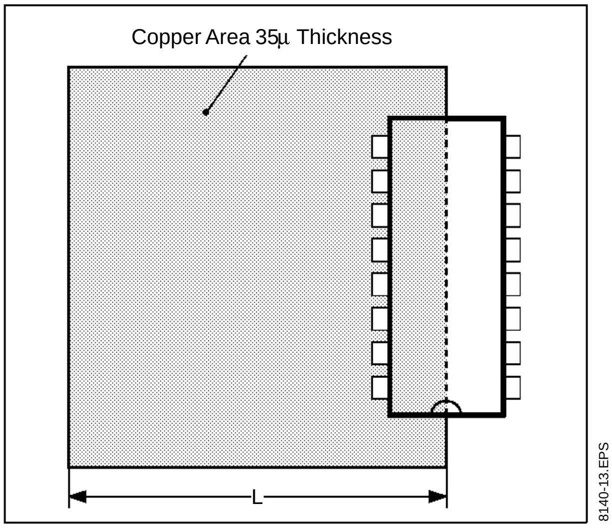
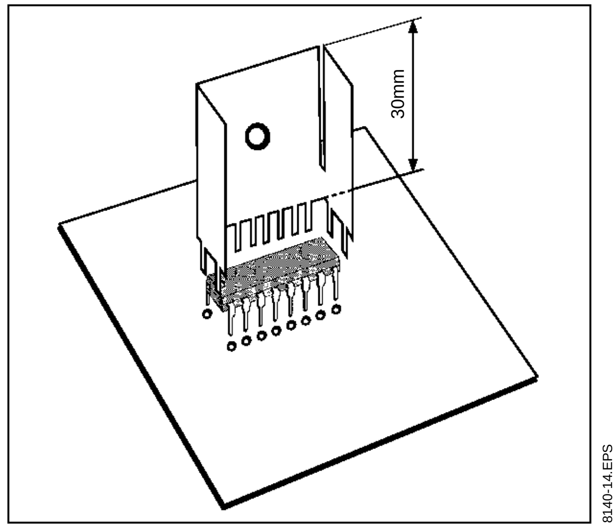
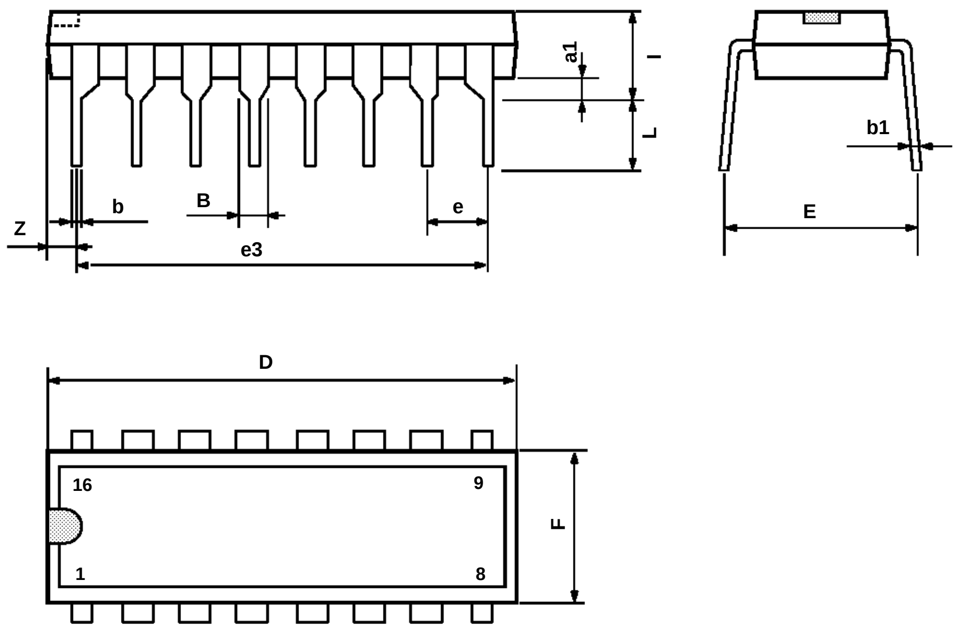


Figure 11 : Example of an External Heatsink



PACKAGE MECHANICAL DATA

16 PINS - PLASTIC POWERDIP



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			20			0.787
E		8.8			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

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